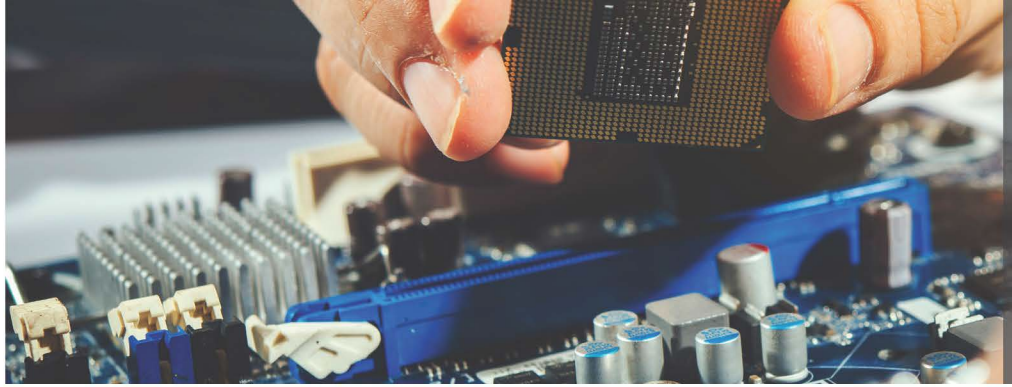
PLUNIFY

Optimise Semiconductor Chip Placement with Machine Learning

Plunify helps semiconductor design engineers improve design performance, and save time and resources in the design process.

Started in 2009 by two passionate engineers, Plunify optimises chip design performance and creates innovative solutions to accelerate product time-to-market.

Plunify has operations in Singapore, Malaysia, Japan and in the US.



"The team from AISG provided much-needed expertise and diligence to help us design and craft the data pipeline and models for this effort – vital to this project's success."

Ng Harnhua, Co-Founder, VP of Engineering

BACKGROUND

- Both FPGA and ASIC chips are widely used in consumer electronics as well as in enterprise systems. Each chip typically consists of hundreds to millions of transistors (depending on size and complexity)
- Chip placement is the process of arranging different modules on a chip before manufacture. It is a laborious step (takes days to weeks)
- Due to modern chip complexity, finding optimal placements require highly experienced engineers.
- Poor chip placement leads to the product not meeting performance specifications, incurring costly delays in the production schedule

BUSINESS CHALLENGE

How can Plunify speed up the chip design process using AI?

AI SOLUTION DEPLOYED

AI technologies, aimed at assisting human experts, are used to speed up the chip placement process

- A chip placement consists of rectangular grids, with each grid containing parts of one or more modules
- Convolutional neural networks and other deep learning architectures were used to improve the quality of chip placement by predicting good and bad placements with high accuracy
- Computationally-efficient generative models were used to generate chip placements; AI models were used to predict good ones for production

OUTCOMES

Shortened product development cycle for Plunify's chip design partner companies from 2 months to a week, including:
- *Power chips used in automotives;*
- *Communications chips used in 5G Internet*

New technological breakthrough in applying image recognition on chip placement with **80%** accuracy

Decreased prototyping cost of new chips by **8%**

10x less development time for new chip designs